High-Performance Heterogeneous Computing Platform “GRIFON”
Input, processing and analysis of large volumes of radar and visual data.

High resolution imaging and creation of virtual reality systems.

Ensuring efficient operation of distributed real-time databases and data storage systems.

Application for parts of the combat information and control system.
Bus-structured modular system based on Compact PCI Serial specification with 3U modules in size
Heterogeneous: use of computers with various architectures:

1). CPU modules with x86;
2). Computers based on graphics processors (Nvidia, AMD);
3). Computers based on FPGA (Virtex, Kintex).
Parallel-pipeline computational process and scalability at the level of modules and units
Computing platform contains:
<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPC512</td>
<td>3U Intel Core i7 3rd, 2/4 cores, DDR3 8GB</td>
</tr>
</tbody>
</table>
# FPGA-based computers

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPU500</td>
<td>3U VIRTEX-6, RAM 4 GB DDR3, FMC HPC, PCIe x8 Gen3</td>
</tr>
</tbody>
</table>

# Computers based on graphics processors

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIM556</td>
<td>3U GPU Nvidia Quadro K2100M 2GB, 576 Cores TDP 55W, PCIe x8, 750Gflops SP</td>
</tr>
<tr>
<td>VIM556-03</td>
<td>3U GPU AMD Radeon E8860 2GB, 640 Cores TDP 55W, PCIe x8, 768Gflops SP</td>
</tr>
</tbody>
</table>
### Switches and extenders

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>KIC551</td>
<td>3U Switch PCIe/10 Gbit Ethernet, PCIe Gen3, Fiber Optic</td>
</tr>
<tr>
<td>KIC552</td>
<td>3U Extension Module PCIe Gen 3.0 x8 Fiber Optic 50 m</td>
</tr>
</tbody>
</table>

### I/O Modules

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIC551</td>
<td>3U PCI-E x1, 2x mezzanines with I/O (RS485/422/232, digital I/O, analog i/o, current loop, CAN, MIL STD1553)</td>
</tr>
</tbody>
</table>
Interaction Structure for Units of GRIFON High-Performance Heterogeneous Computing Platform

- CPC512
  - CPU
  - Interface between CPU and PCIe buses
  - PCIe - GEN 3.0 switch with integrated DMA controller

- CPC512
  - CPU
  - Interface between CPU and PCIe buses
  - PCIe - GEN 3.0 switch with integrated DMA controller

- NTB

- KIC551
  - 10 Gbit Ethernet
  - Controller for PCIe bus extension
  - PCIe - GEN 3.0 switch

- DIC551
- CPU/GPU/FPU (x4)
  - PCIe Gen3
  - PCIe Gen3
  - PCIe Gen3

- KIC552
- CPU/GPU/FPU (x4)
Inter-Modular Interaction Mechanisms

**CPU-CPU**
- Network driver with the transferring over PCIe.
- Library that displays memory parts of one module to the other.

**CPU-FPGA**
- Set of cores and their drivers, organizing interactions.

**CPU-GPU**
- CUDA SDK operation.

Support of peer-to-peer interaction between computing modules
Implementation as per requirements for resistance to external influencing factors in accordance with the GOST RV 20.39.304-98
Unit Scalability

- Set of modules depends on a particular task
- Bandwidth between any pair of modules is up to 32Gb/sec.
System Scalability

- Various topologies of inter-unit connections with the use of PCIe.
- Bandwidth up to 32 Gb/sec.
- With the use of 10 Gb Ethernet.
Parallel-Pipeline Data Processing
As exemplified by the system of high-definition video processing in real-time

CPC512 – host
FPU500 + 3G-SDI Mezzanine board
KIC551 - PCIe-switch
VIM556 – 4 pcs
KIC550 – HDD storage
Full-HD cameras - 4 pcs
Example of the Autonomous Distributed Database

GRIFON configuration:

KIC551 – 1 pcs.
CPC512 – 4 pcs.
KIC550 – 4 pcs.
Parallel-Pipeline Data-Processing
as exemplified by mobile system of data acquisition and processing for wireless communication channels

**GRIFON Configuration:**

FPU500 + mezzanine board
CPC512 - host
CPC512 – data processors 2 pcs
CPC512 – contextual search 2 pcs
KIC551 - PCIe-switch
KIC550 – HDD storage
Activated / Deactivated Functions

- 1 – Detection of faces
- 2 – Recognition of faces
- 3 – Determination of distances to objects
- 4 – Detection of movements
- 5 – Keeping track of the object highlighted by mouse
- 6 – Detection of people
- 7 – Detecting any objects (interacting with user via appropriate algorithm)
Continuously Repeatable Data Processing Cycle

- Receiving frames from 8 video cameras
- Linking panoramic sight for the left and right eye from the frames of 8 video cameras
- Drawing up a map of distances for any frame point
- Face detection HaarCascades (if LBP face detection is activated)
- Searching for moving objects
- People recognition (HOG method)
- Detecting movements of mouse-highlighted objects
- Detecting any objects (interacting with user via appropriate algorithm)
- Displaying new frames on the screen of 3D-monitor
- Displaying frames in 3D Virtual-Reality Headset Oculus Rift Dk2
- Compression of the current video-frame in H264-mpeg format using the hardware ASIC-codec nVidia
Performance Characteristics

- Speed of linking frames from 8 video cameras to the Full-HD 1920x1080 stereo-panorama without blurring, at 1 GPU – 12 FPS, response 100 ms.
- Displaying speed in the Oculus Rift Full-HD headset – 65 FPS, response 15 ms.
- Speed of face recognition on panorama – 4 FPS, response 250 ms.
- Speed of recognition of 10 faces from the data base of 100 faces – 4 FPS, response 250 ms.
- Speed of keeping track over the highlighted object at GPU (PyrLK Optical Flow 150-200 FPS), but it is limited by the panorama linking speed - 12 FPS, response 100 ms.
- Speed of generation of distance map using GPU and defining distances to the objects – 3 FPS, response 300 ms.
- Speed of building 3D model in the territory in sight – 1 FPS, response 1 second.
- Speed of movement by the 3D model, using integrated graphics CPU – 20 FPS, response 50 ms.
Contact US

FASTWEL Group Co. Ltd
108 Profsoyuznaya St.
Moscow, 117437 Russia
Tel: +7-495-232-16-81
Fax: +7 (495) 232-1654
E-mail: info@fastwel.com
Url: www.fastwel.com